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High Efficient CSDG MOSFET based Boost Switching Regulator

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ABSTRACT: This research work proposes a boost regulator, using the novel Cylindrical Surrounding Double-Gate (CSDG) Metal Oxide Semiconductor Field-effect Transistor (MOSFET) device as the switching device. This circuit is suitable for dc-dc power converter and for low input voltage devices (<*1 V*). This device is peculiar due to its downscaling for nanotechnology applications. This attribute makes it possible to scale its channel length up to about *3 nm*, making it applicable in Very-large-scale integration (VLSI) technology and low power input devices. Using this device, it has been observed that better physical size, higher efficiency, and high conversion ratio is achieved, and helpful in boosting devices of low input voltage.

Keywords: Boost regulator, CSDG MOSFET, dc-dc converter, Efficiency, Microelectronics, Nanotechnology, Power management, Switch, VLSI.

Abbreviations: CSDG, cylindrical surrounding double-gate; DG, double-gate; LED, light-emitting diode; LCD, light crystal display; MOSFET, metal oxide semiconductor field-effect transistor; SG, single-gate; VLSI, very-large-scale integration.

I. INTRODUCTION

The transfer of energy from one level to the other is required in electrical and electronic transmission applications, and this is made possible using the switch. The dc-dc voltage regulator is widely used in domestic appliances, which require Light Emitting Diode (LED) drivers and Light Crystal Display (LCD) circuits such as TVs and mobile phones [1]. This is possible because of the fewer external components required in reducing the size of the devices. The regulators are also applicable in industrial automobiles such as forklift trucks, trolley vehicles, and electric automobiles [2]. The energy transfer concept is made through the inductor and capacitor components with reduced power losses [3]. Due to the fast switching speed and input impedance coupled with other advantages, the Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) has proved itself to be an essential part of the electronics configuration. With these advantages, it is relevant to devices of low current to perform optimally [4].

The MOSFET, a switching device, has been appreciated due to high efficiency, fast frequency response, and good acceleration control the linear and boost regulator has been realized by Srivastava *et al.*, [3, 5]. However, due to the transistor's dynamics, different types of MOSFETs and configurations have been employed in the switching property of the boost regulator. Also, to create a multi-gate MOSFET with each gate having different work functions, a new DG MOSFET was introduced [6]. This structure provided an increase in transconductance and suppressed SCE as compared with Single-Gate (SG) MOSFET. In addition, this structure is also good for application due to its increased lifetime in operation and gate transport efficiency [7]. One of the major setbacks is that the constant oscillatory frequency current control is the subharmonic oscillation within the ON-state and OFF-state [6]. Various research works solve this challenge by introducing the inductor current slope compensation and 1-D staircase effect etc. [8-13].

However, the slope compensation tends to complicate the configuration and core purpose of the boost regulator. This is because either way, when the compensation is not sufficient, the fluctuation in the flow of current in the design cause instability to the system. At the same time, oversupply of slope compensation affects the current mode control of the system. Also, Ahmed *et al.,* [14] have proposed a model for increasing the current control for the system. In this work, 0.5 µm industry-standard CMOS devices were utilized with comparators and inductors simulated to produce a linearly increased output reference. The output reference shows a smooth dc-dc controlled system without discontinuity or compensation at any point in the system. Although the circuit system requires quite a few components that do not compensate for the scalability and cost-effectiveness, the circuit may be trying to accomplish.

Singha *et al.,* [15] proposed a theory of numerical prediction as well as experimental analysis into the instabilities that occur in the boost regulator-controlled system. This was performed using discrete-time models in the form of 1-D non-continuity plot. In this work, a staircase effect was utilized to compensate for the sub-harmonic compensation, which helps to meet the quantization requirement [16]. The predictive and analytical framework may also be applicable for nonlinear current control for the dc-dc boost regulator. Due to limitations in the system's switching and

oscillation, this work will be investigating the application of a novel MOSFET device in the dc-dc boost regulator system. Also, an integrated digital low-dropout regulator was proposed for controlling time-coding events [17]. The work was successful in this aspect as off-chip capacitors are being scaled to compensate for changes in load current during operations. However, this approach encounters difficulty with a sub-1V supply voltage as it results in increased power dissipation due to high-frequency clocking [18]. Literature has been written to prove these observations using other transistor types, but the CSDG MOSFET proves to have better efficiency. This research work is organized as follows: The building blocks used to assemble the boost regulator have been discussed in Section II. The proposed model of CSDG MOSFET based boost switching regulator has been described in Section III. Section IV discusses the efficiency analysis of the CSDG MOSFET based boost switching regulator. Finally, Section V concludes the work and Section VI, recommends the future works.

II. BASIC BUILDING BLOCKS USED IN THIS ANALYSIS

In building the CSDG MOSFET-based boost regulator, the following building blocks are being discussed as structural modeling of the CSDG MOSFET and application of the CSDG MOSFET Boost switching regulator.

A. CSDG MOSFET

Due to scalability employed in Nanotechnology, multi-gate MOSFET has been utilized in electronic applications. Double-gate (DG), FinFET, and surrounding-gate MOSFETs have benefited immensely on the large-scale application [19-22]. However, using the CSDG MOSFET as an extension of DG MOSFET helps to better control the channels using the dual-gate. This helps to effectively suppress the Short Channel Effect (SCE) while aiding better drain current in its application [23]. Two Single-Gate (SG) MOSFET arranged back-to-back to each other with one of its gates revolving around the second one, which acts as a pivot represent the CSDG MOSFET as shown in Fig. 1.
In this device, the inner channel has identical properties as external channel, such as the thickness, width, and doping properties. For the independent activity, a thick substrate is used to separate the two channels. The blue color represents the two gates, while the oxide that serves as a dielectric between the gates the channel is represented with yellow color [24]. When an applicable positive voltage is applied at the gates of the n-channel enhancement CSDG MOSFET, the body which has holes as its majority carrier will begin to have holes repelling from the insulating oxide and the electrons (minority carrier) attracted toward the gates [25]. This activity aids the easy migration of the electron at the n-type substrate from the device's source to the drain. This migration creates an n-type channel at the upper part of the p-type body. This novel structure is different from other similar structures by an intruding drain and the source region. This effect is advantageous in overcoming punch-through effect, velocity saturation, and SCE. Also, a hollow situated at the vertical center of the structure helps combat some heating effect associated with its performance.

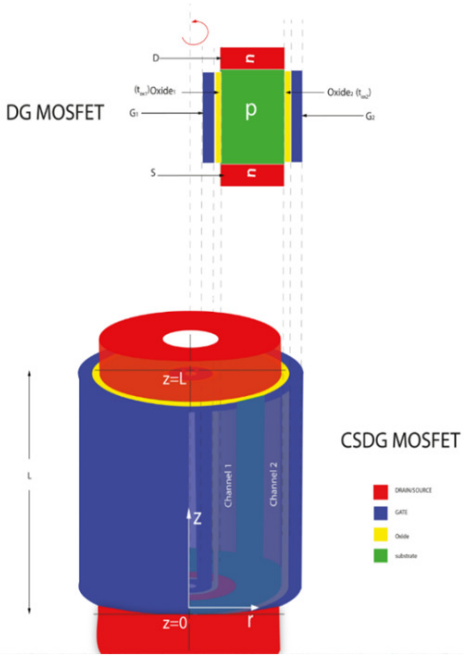

Fig. 1. The n-channel MOSFET [24].

The peculiarity in the downscaling of the CSDG MOSFET in nanotechnology applications makes it possible to scale its channel length up to about *3 nm*, making it applicable in VLSI technology and low power input devices. The CSDG MOSFET, like other transistor types, can be used as a switch such that the device is at OFF-state when the input voltage is below the threshold voltage, and ON-state when it is above the threshold voltage. The CSDG MOSFET enjoys low threshold voltage characteristics, hence a suitable ON-resistance for low power consumption devices.

B. Boost Switching Regulator

The switch-mode regulator helps to step up lower voltage into a higher voltage at a fast speed [26]. When the input voltage (V_{in}) is passed through the magnetic inductor (L) in Fig. 2, the inductor magnetic field starts to collapse and thus induce current, resulting in a high voltage spike in the circuit. Knowingly well that the energy stored in an inductor is given by [27]:

$$\frac{1}{2}\times L_o \times I^2 \quad (1)$$

where L_o is the inductance of the coil, and I is the maximum peak current. At this instant, energy is stored in the inductor from the input voltage, and it is transferred at a higher voltage, allowing for the conservation of power. This continuously happens in about a thousand times in a second (depending on the switching oscillation), and so the energy adds up in every cycle to get a nice measurable and useful energy output [28].
The Switch (S), when turn-ON, allows the current flows from the inductor through the switch back to the input voltage. However, when the switch is turn-OFF, current no longer flows through its paths and thus allows more

collapse of the magnetic field in the inductor such that a higher voltage spike allows current to pass to the diode through the capacitor in parallel [29]. The output capacitor is now charged to a higher voltage than before, which implies that it has been successfully stepped up from a low DC voltage to a higher one.

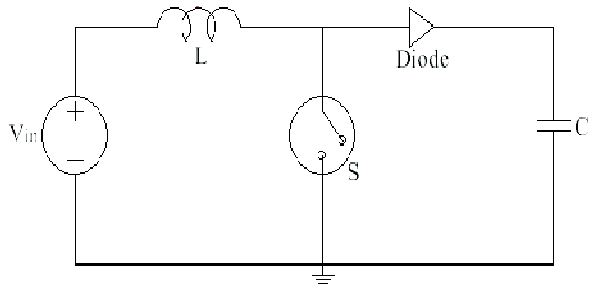

Fig. 2. The basic boost circuit.

As this oscillation occurs, the current is stored at the capacitor and discharged when the switch is turn-ON, and the diode (as a passive switch) helps prevent the reverse flow of the current to the voltage source. Also, due to the fast switching in the circuit, the inductor's magnetic field does not fully collapse (but polarity change to accommodate the flow of current), so when the switch is turned-ON again, more voltage is formed in the process [30]. The output voltage of the circuit can be controlled through the percentage of time the switch in turn-ON, hereby, mathematically expressed as [31]:

$$V_{out} = \frac{V_{in}}{1-D} \tag{2}$$

where D and V_{out} are the duty cycle and output voltage, respectively, Inductor-based regulator such as in Fig. 2 achieves higher step-up voltage gain through fine-tuning the turn ratios [32, 33]. However, there is deterioration in the conversion efficiency because of the induction's stored energy that caused the voltage spike in the switch. But to overcome this challenge, an active-clamp circuit configuration was added to the inductor-based regulator [34]. This was aided with a single-switch [35-41] introduced in some literature to combat the challenges. However, one thing was obvious in all these, the conversion ratio remains limited. This initiates a CSDG MOSFET based boost regulation where the double-gate transistor device controls the circuit.

III. PROPOSED MODEL OF CSDG MOSFET BASED BOOST REGULATOR

For the proposed CSDG MOSFET based Boost regulator (Fig. 3), the output voltage is higher than the input voltage. Since the circuit is expected to store some energy from the input and transfer that same energy to the output, though, at a higher voltage, power is conserved. The two gates of the CSDG MOSFET are used as the switch [42]. This circuit stores more energy as the transistor device consists of two independent MOSFET operations that apply to both switches.

The coupling inductor L in Fig. 3 is assumed to be part of an ideal transformer of which the input voltage is introduced. Also, the dead time between the two channels of the CSDG MOSFET is not significant in this circuit configuration. Thus, the CSDG MOSFET switch and the diode device are assumed to be ideal. Moreover, the capacitors, C_{out} is assumed to be large enough to store a constant voltage across it during the operation, and the switching ripple magnitude negligible.

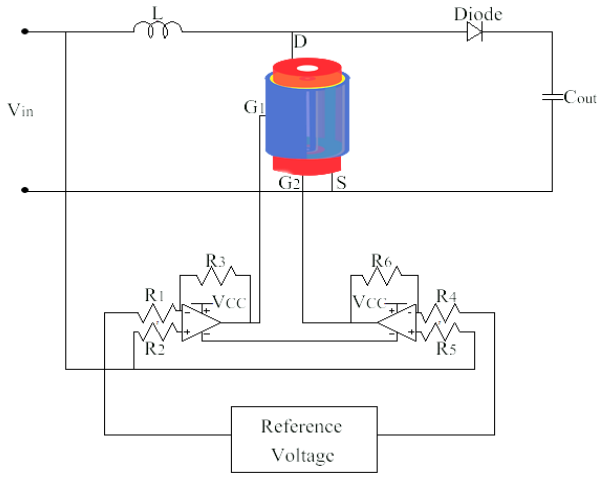

Fig. 3. The proposed SCDG MOSFET based boost regulator.

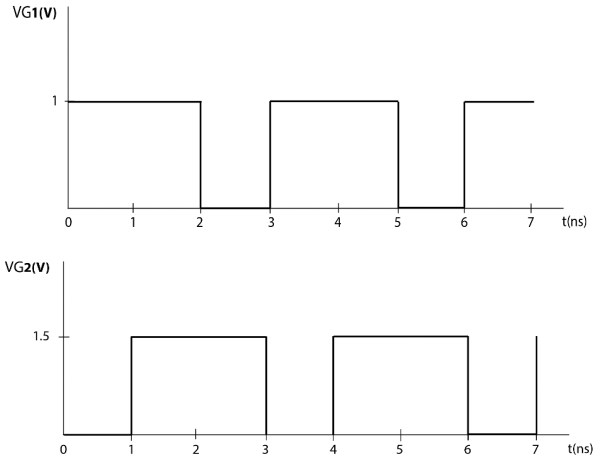

Fig. 4. Switching sequence of both switches in the proposed regulator.

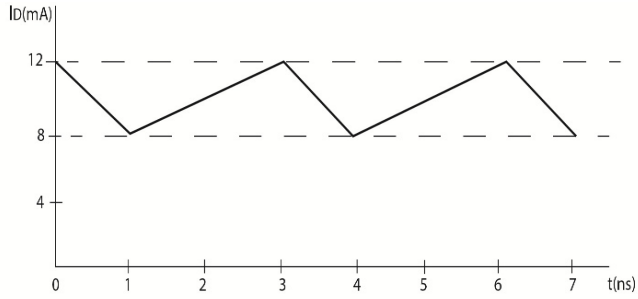

Fig. 5. The total current in proposed regulator.

This assumption is based on applying Meyer's model. The CSDG MOSFET proves to be of better capacitance [43]. The total capacitance in series and parallel as drain-source current flow through it is expressed as:

$$C_{CSDG} = C_{ox1} + C_{DS1} + C_{DS2} + C_{ox2} + \frac{C_{GS1}.C_{DG1}}{C_{GS1}+C_{DG1}} + \frac{C_{GS2}.C_{DG2}}{C_{GS2}+C_{DG2}} \quad (3)$$

The C_{GS1} and C_{GS2} are the gate-source capacitance of the inner radius and gate-source capacitance of the outer radius, respectively. While C_{DG1} and C_{DG2} are the gate-drain capacitance of the inner radius and gate-drain capacitance of the outer radius, respectively. The drain-source capacitance of the inner radius (C_{DS1}) and drain-source capacitance of the external radius (C_{DS2}) also complement the high capacitance. Also, C_{ox1} and C_{ox2} are the oxide capacitance of the inner radius and the oxide capacitance of the outer radius, respectively.

Due to the two independent channels created in the CSDG MOSFET, thus there are two independent modes in the proposed circuit configuration. The dual-gate of the CSDG MOSFET devices are triggers for voltages V_{GS1} and V_{GS2}, respectively. These serve as the two switches in the circuits about duty circles *D* and *(1-D)*, respectively. The input current is denoted by I_{in}, and the current flows from inductor *L* as I_L while the voltage through it as V_L. When the switch G_1 is triggered with a threshold of 0.7 V, there is a current flow along its channel shown in Fig. 4a. This process is replicated in channel-2 when switch-2 is triggered at *1.5 V* as shown in Fig. 4b. The schematic of the synchronous boost regulator with CSDG MOSFET is shown in Fig. 3. The circuit consists of two main building blocks: (i) Comparator based controller, (ii) synchronous boost regulator [3, 15, 33, 44]. The boost regulator is controlled by reference voltage signals generated from the ultra-low-power comparators. A secondary voltage cell is used to obtain a reference open-circuit voltage V_{ref} to set the theoretical V_{GS1} and V_{GS2}.

IV. EFFICIENCY ANALYSIS

Over the decades, efficiency as basic power regulator parameters for a circuit such as a buck, boost, and the boost-buck regulator has been established [45]. This research work focuses on the calculation of efficiency for circuits with low input voltage. The input voltage is taken to be less than 1 V while efficient is of high demand. However, the majority of the losses in this circuit are within the inductor and the CSDG MOSFET. The inductor and switch losses affect the efficiency of the CSDG MOSFET based boost regulator. However, in order to achieve effective efficiency, these losses are not being considered. The efficiency of the basic circuit is:

$$\eta = \frac{P_{out}}{V_{in} I_{in}} \times 100\% \quad (4)$$

while the duty ratio of the basic circuit is also expressed as [44]:

$$D = \frac{1 - V_{in}.\eta}{V_{out}} \quad (5)$$

From Eq. (5), the duty ratio of the CSDG MOSFET based boost regulator is expressed as:

$$D_{CSDG} = \frac{I_D r_L - (V_1 + V_2)}{I_D r_L} \quad (6)$$

Applying the drift-diffusion model to drain current along the two channels is expressed as [5]:

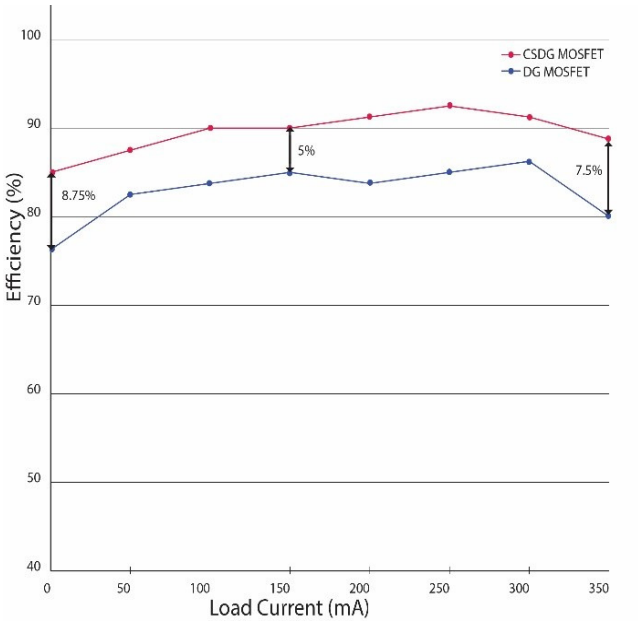

Fig. 6. The proposed regulator's efficiency compared with the DG MOSFET-based boost regulator.

$$\int_0^L I_{d1} dL = 2\pi(a+b) \int_{\psi_{s0}}^{\psi_{sL}} \mu_s(-Q')d\psi_s + \Phi 2\pi(a+b) \int_{Q'_0}^{Q'_L} \mu dQ' \quad (7)$$

where *L* and *Q* are the channel length and charge, respectively. The surface potential of along the length is represented by $\psi_{sL}$and ψ_{s0}respectively, while μ_s and Φ_t are the carrier mobility and thermal voltage, respectively. Q'_L and Q'_0 are the charges along the channel length, and then I_d is the drain current in the CSDG MOSFET boost regulator expressed as:

$$I_{d_{CSDG}} = \frac{2\pi(a+b)}{L} \mu_s \begin{bmatrix} 2C_{ox}\left(V_{GS_{total}} - V_{FB}\right) - \\ C_{ox}\left(\psi_{sL} + \psi_{s0}\right) + 2Q_B + \\ \left(2\Phi_t C_{ox} - Q_B\right) \end{bmatrix} \quad (8)$$

where *a* and *b* are the radii of the inner and outer gates, respectively, $\mu_S$and C_{ox} are the mobility of the electron flow within the channel and the oxide capacitance, respectively. The $V_{GStotal}$ and V_f are the total voltages applied at the gates (V_1+V_2) and feedback voltages, respectively. Applying Eq. (5) into Eq. (2) will produce:

$$V_{out} = \frac{V_{in}}{1 - \left[\frac{I_d I_r - (V_1 + V_2)}{I_d I_r}\right]} \quad (9)$$

$$\eta = \frac{\frac{V_{in}}{1 - \left[\frac{I_d I_r - (V_1 + V_2)}{I_d I_r}\right]}}{V_{in} I_{in}} \times 100\% \quad (10)$$

Substituting Eq. (9) into Eq. (4), the efficiency of the CSDG MOSFET boost system configuration is expressed in Eq. (10). This is numerical analyzed and compared with the DG MOSFET from other literature as shown in Fig. 6.

Comparing the proposed CSDG MOSFET-based boost regulator's efficiency with the DG MOSFET boost regulator, as shown in Fig. 6 [3]. It is observed that the CSDG MOSFET operates at a higher switching speed due to its cylindrical structure, which could also reduce the switching losses encounter in the regulator. Also, it is observed that at low load current in the circuit, the efficiency is about 8.75 % higher, while 5% at an average load current and 7.5 % higher at high load current, using the CSDG MOSFET as a switch than the DG MOSFET.

V. CONCLUSIONS

In this research work, the CSDG MOSFET was utilized to model a circuit configuration for better and higher efficiency for boost regulator. This circuit has proved to have a better switching speed and provides an almost double drain current than the double-gate MOSFET. This helps the circuit to provide a higher output voltage. The application of this circuit can be utilized in the power system management of many electronic devices and any device with the dc-dc conversion.

VI. FUTURE

In the future, this work can be focused on the conduction and switching losses in the circuit with the noise associated with them.Also, the configuration of the CSDG MOSFET with another regulator e,g, buck and buck-boost topology can be considered.

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Conflict of Interest. Authors confirm that there is no conflict of interest.

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